Design and Verification of 16nm FFC Low Power SerDes for Datacenter and Automotive Applications

Mentor Graphics / Analog Bits

ABSTRACT

SerDes technology is removing datacenter communication bottlenecks and transforming the way we visualize and virtualize information. SerDes increases the bandwidth of very large data transmission from server to server, switch to switch, and server to storage. There are typically 1 million links that are constantly on and as many as 100 SerDes per SoC in today's leading designs. At the same time, SerDes technology is being used in automotive applications, enabling higher performance at lower cost, smaller footprint, and reduced power consumption. Automotive applications typically require additional characteristics such as grade 1 quality (-40°C - +125°C) and high-reliability.

In order to achieve the stringent power, performance and area requirements for these diverse applications, three major components have to come together to enable success: (1) the multi-protocol SerDes architecture that delivers low power, the required data rates, and the required jitter; (2) the process technology that enables the performance power and area requirements; and (3) the circuit verification platform that ensures that the IP will operate as expected across all operating, environmental, and process conditions.

As an example of such success, this presentation describes the design, verification, and silicon data performance of an Analog Bits Low Power 1-22G PCIe Gen4 / SAS4 PHY SerDes fabricated in TSMC 16FFC process technology and verified using the Mentor Graphics Analog FastSPICE Platform.

The TSMC 16FFC process technology delivers significant advantages in power, performance, and area compared to existing 16FF processes. This process technology - coupled with a breakthrough low-power architecture- enables the SerDes to achieve 130mW per lane at 22.5Gbps (5.8mW/Gbps) and 96mW per lane at 16 Gbps (6mW/Gbps). The IP has a compact form factor of 0.145 mm2 total active area per lane and multiple orientations enabling placement anywhere on the SoC. The design exhibits exceptional input sensitivity, input jitter tolerance and low output jitter. The Tx jitter max (Rj-rms, Tj @16Gbps BER 1e-12) is RJ=0.7ps and Tj=13.8ps.

The circuit verification methodology used to ensure the design meets spec and complete the jitter analysis relies on Mentor Graphics Analog FastSPICE (AFS) Platform and includes analysis of all device noise contributions, sensitivity analysis, RC parasitics, PVT and mismatch variations. With AFS, the design team was able to simulate the SerDes at the full-circuit level, including the effects of device noise and parasitics, ensuring very high confidence before tapeout. The AFS Platform is certified in the TSMC SPICE Qualification Program, and AFS Full-Spectrum device noise analysis is validated in the TSMC Custom Design Reference Flow.

In this presentation, we first review the design requirements for the low power SerDes IP and the corresponding requirements on the high-performance PLL to meet the stringent jitter specifications. We describe the key effects that must be captured in any analysis to provide an estimate of the phase noise and jitter expected in TSMC 16nm FFC technology. These include the impact of device noise, the identification of the top noise contributors, the capture of all post-layout effects, comprehensive PVT, and mismatch analysis using the AFS Platform. We then present silicon-data results for eye diagram, phase noise, and jitter analysis and illustrate the excellent correlation with the AFS Platform full-circuit SerDes verification.

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Ravi Subramanian – Mentor Graphics
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Introduction

Presenting circuit verification results of 16nm FFC Low Power SerDes

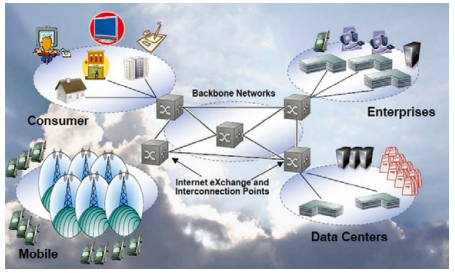
- Three way collaboration between:
  - Analog Bits: 16nm FFC Low Power SerDes IP
  - TSMC: 16nm FFC Process and Reference Flows
  - Mentor: AFS Platform circuit verification and noise analysis

Open Innovation Platform®

Outline

- SerDes Demands
- Analog Bits Overview
- 16nm FFC Half Power SERDES at PCI Gen4 Data Rate
- SerDes Verification Challenges
- Analog FastSPICE (AFS) Platform Overview
- Simulation and Silicon Results
- Summary

High Speed I/O Demands

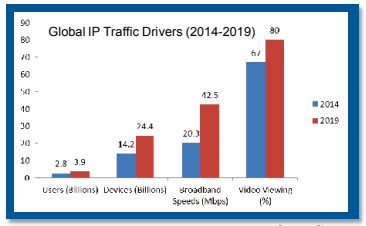


Source: 400Gb/s Call-for-interest

Key Applications Are Driving IP Demand

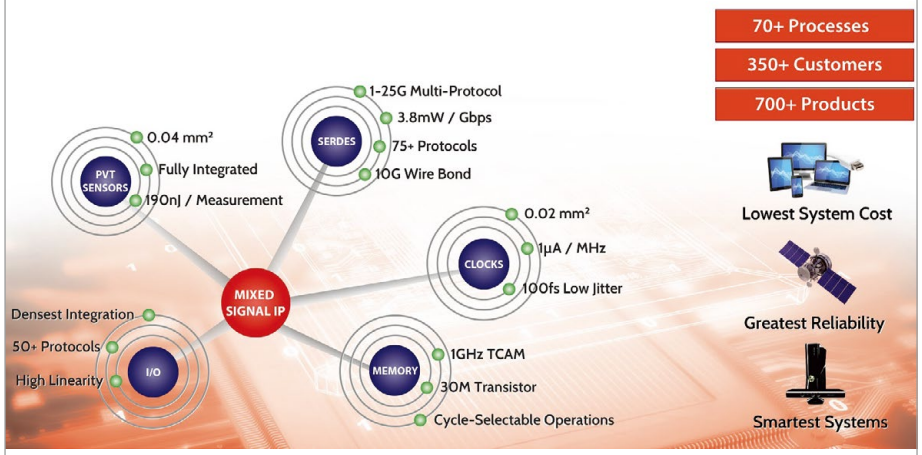
Increasing connectivity demand

- Consumer applications
  - YouTube, Facebook, Amazon, Netflix
  - Smartphones, IoT
- Cloud Computing
- Automotive
- Government and Business
  - Weather predictions, Financial analysis
  - Genomics research, Design simulation



Source: Cisco

Broadest Portfolio of Differentiated IP
Billions in Silicon



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Analog Bits Low-Power, Multi-Protocol SERDES

- Multi-Rate, Multi-Protocol SERDES
  - Lowest power & latency
  - Smallest area
  - Programmable for numerous channel environments
- And enabling many SOC applications

Wearables

FPGA

Consumer Cables

Mobile Computing

Supercomputers & Communications

Flat Panel Display

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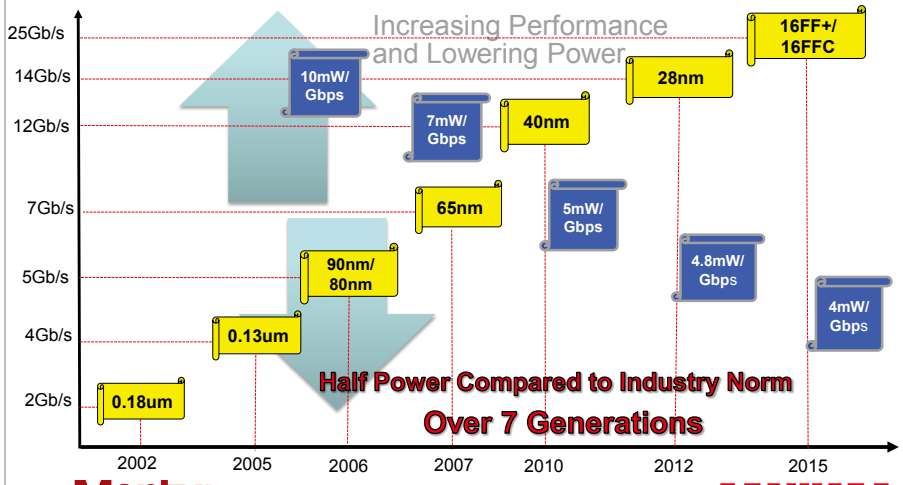
2 Decades of Low Power SERDES Track Record
1st Time Right in over 16 processes including 16nm



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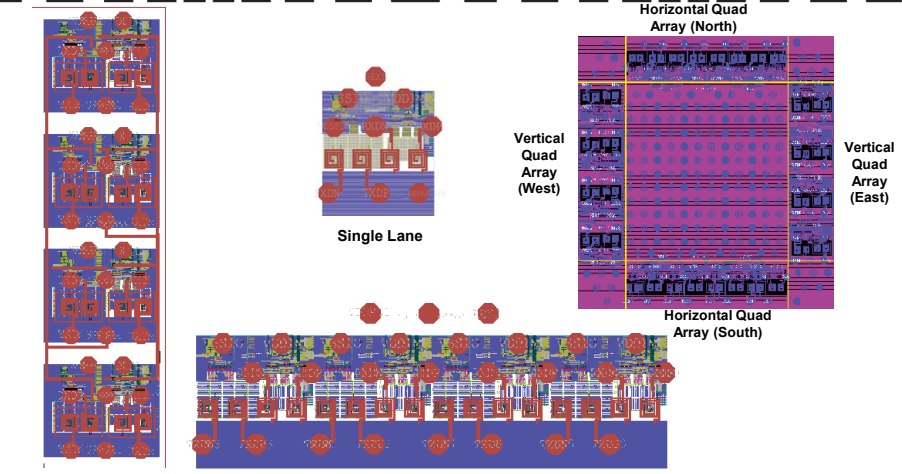
Fully Integrated, Flexible with Multiple Orientations
allows SERDES to be placed anywhere on SOC



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Higher Reliability Requirements for SERDES

- Dictated by automotive and datacenter applications
- Need Reliability/Aging Simulations
- AEC-Q100 Grade 2 Qualifications
  - High Temperature Requirements
  - Special ESD tests needed

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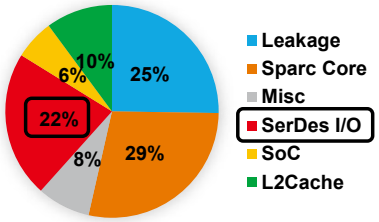
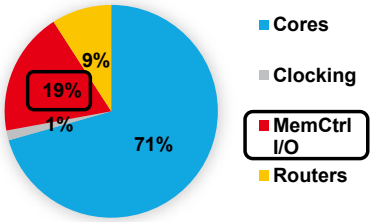
The SerDes Low-Power Challenge

16 Core SPARC Processor



[1]

48 Core Intel Processor

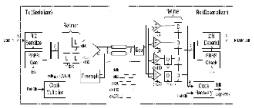


[2]

Serial links consume ≈20% of processor power*

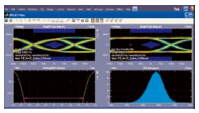
Challenges to Matching Silicon

Simulated Circuit



Uncertainty

Measured Silicon



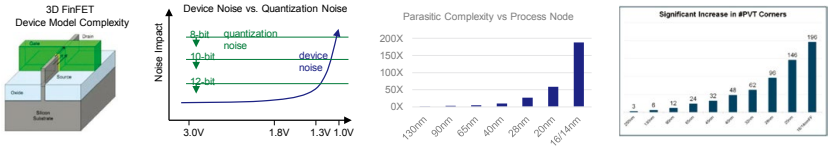
Simulation Uncertainty

- Model accuracy (SPICE, variation, corners)
- Process variation (global & local)
- Parasitic devices (extraction, variation)
- Layout effects
- Thermal effects
- Device noise, noise bandwidth, runtime
- Circuit simulator accuracy (noise floor)
- Distribution uncertainty (sample size)
- Measurement post-processing

Measurement Uncertainty

- Specific silicon manufacturing
- Lot, wafer, and die selection
- Specific contextual circuit activity
- Test equipment (method and resolution)
- Probe effects & variability
- Temperature & variation
- Voltage & variation
- Distribution uncertainty (sample size)
- Measurement post-processing

First Order Nanometer Physical Effects



- Technology Perspective:
  - Need to include device noise effects
  - Need to include huge number of parasitics
  - Need to include impact of lossy channels
  - Increasing device model complexity for FinFET
  - Complex layout effects impacting design specs
- Design Perspective:
  - Reinventing designs for low-supply-voltages
  - Low power applications for analog IP
  - Fully SPICE accurate simulation with very low noise floor
  - Need Monte Carlo and many corners to ensure operation

- Huge netlists
- Longer Simulations
- Lots of Simulations
- Device Noise Required

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AFS Platform Quick Overview

AFS Mega
- Embedded SRAM Characterization
- Compatible w/ digital FastSPICE flows
- Accurate power and timing characterization
- Same Performance as less accurate tools

AFS Circuit Simulation
- Foundry certified down to 7nm
- 5x-10x faster vs golden SPICE (1-core)
- 2x-6x faster vs parallel SPICE simulators
- >20M-element capacity

Analog Characterization Environment (ACE)
- High-productivity characterization
- Corner, sweep, and Monte Carlo
- Complex nesting support
- Visual distribution analyzer

AFS AMS
- Easy mixed-signal sim setup
- Runs Verilog and SPICE netlists
- Supports standard Verilog tools
- Leverages AFS differentiation

AFS RF Analyses
- Full-Spectrum periodic noise analysis
- PSS, pnoise, oscnoise, Sampled pnoise
- There is no maxsideband parameter
- >100K element PSS convergence

AFS Transient Noise
- Signoff Accuracy for nm designs
- Must have for PLL, ADC/DAC, High-Speed I/O
- Silicon accuracy for Jitter, Phase Noise, SNDR
- Proven to be within 1–2 dB of silicon

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AFS Device Noise Analyses (DNA)

Circuit Type	Transient Noise	Periodic Noise	Oscillator Noise
Non-Periodic Circuits			
PLLs (int-N and frac-N)	✓		
ADCs (sigma-delta, pipelined, etc.)	✓		
Tx chains and Rx chains	✓		
PHYs and SerDes	✓		
Periodic-Driven Circuits			
Switched-cap filters	✓	✓	
Mixers	✓	✓	
Phase detectors	✓	✓	
Charge pumps	✓	✓	
Dividers	✓	✓	
Periodic-Autonomous Circuits			
VCOs (LC-tank, ring oscillators)	✓		✓
Crystal oscillators (XOs)	✓		✓

Golden reference

Faster with superior diagnostics where applicable

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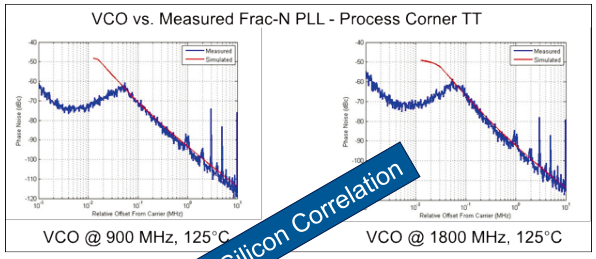
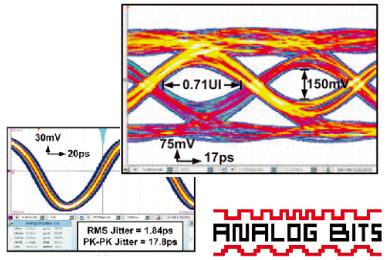
Solving the Verification Challenge with AFS



SerDes PLL

Phase Noise (dBc/Hz)	AFS	Silicon	Difference
PLL Setting 1	-114.8	-114.0	0.8
PLL Setting 2	-114.3	-114.0	0.3
PLL Setting 3	-108.8	-108.0	0.8



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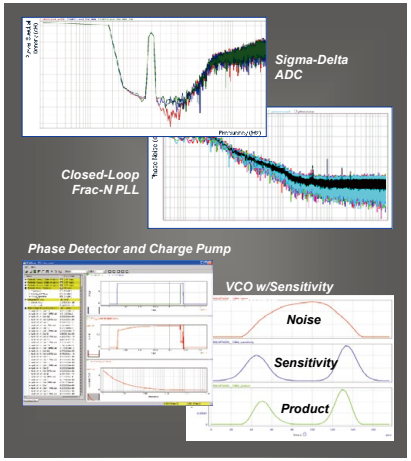
AFS Full-Spectrum Device Noise Analysis



- AFS Full-Spectrum Transient Noise Analysis
  - Transient noise within 1-2dB silicon data
  - Only practical solution for ADCs and PLLs
  - Within 2x AFS runtime (per timestep)
- AFS Full-Spectrum Periodic Noise Analysis
  - Includes all device noise sidebands/harmonics
  - >100K element PSS convergence
  - 5x-10x faster when >100 sidebands
- AFS Full-Spectrum Oscillator Noise Analysis
  - Includes phase and amplitude noise
  - Contribution for every noise source
  - Impulse sensitivity function for every node

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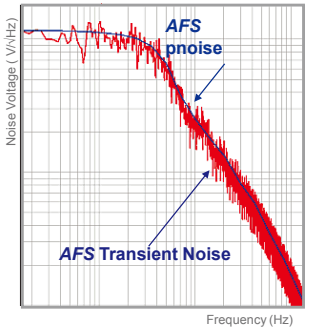
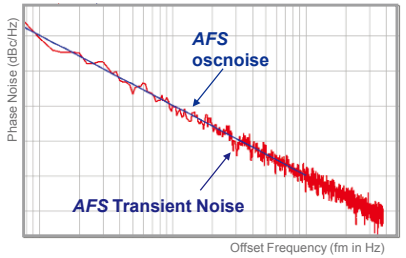
Expect AFS TN and AFS RF Correlation

Full-Spectrum Transient Noise and Periodic Noise Provide Excellent Correlation

Switched-Cap Filter Noise Comparison



4.75GHz LC VCO Noise Comparison



Independent Analyses of the Same Measurement Need to Correlate

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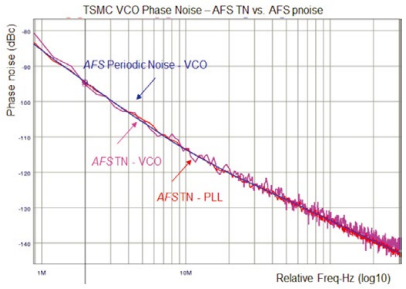
TSMC 20nm Custom Design Reference Flow

AFS Platform Full-Spectrum Device Noise Analysis

AFS Transient Noise Matches AFS pnoise for TSMC PLL



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- Problem: Device noise in analog, mixed-signal, and RF circuits limits performance at 45nm and below
- Solution: Use device noise analysis to characterize performance of analog, mixed-signal, and RF circuits
- Technology: AFS Platform Full-Spectrum Device Noise Analysis for transient noise and periodic noise
- Benefit: Verify PLLs, ADCs, SerDes, and other circuits with nm SPICE accuracy including all device noise effects

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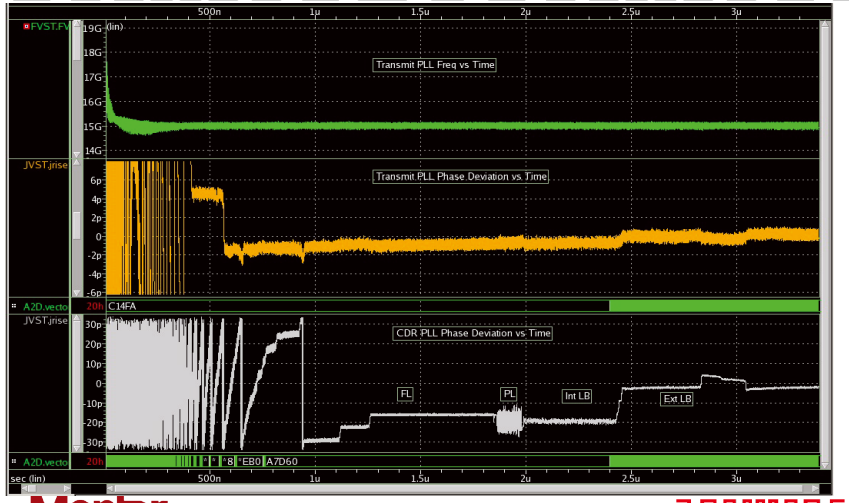
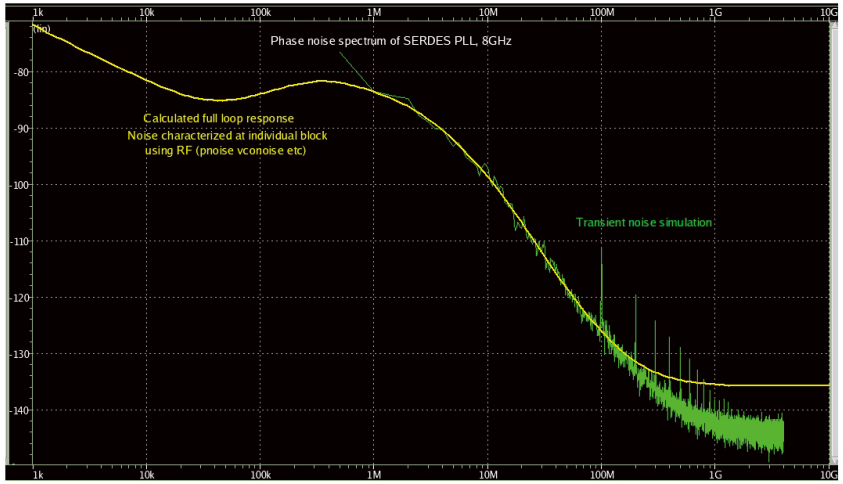
Mentor Graphics Analog Bits Collaboration

- Mentor AFS use on Analog Bits SERDES
  - SERDES - Functional simulation and verification of top-level with parasitic
  - Transient Noise Simulations of PLL/CDR
  - RF/Phase Noise Analysis
- Future work : AFS TMI2 based Aging Simulation

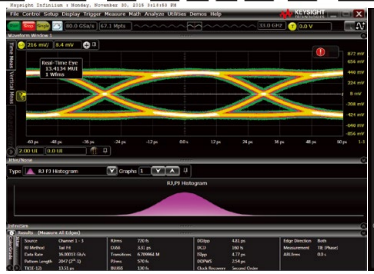
Results of Top Level SERDES



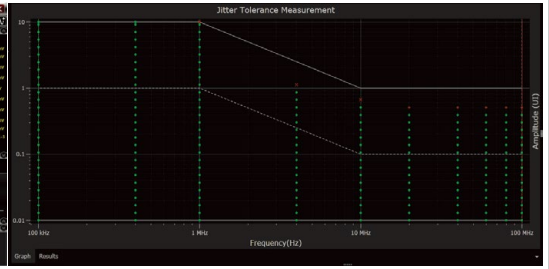
PLL Phase Noise Simulation Results



Half Power SERDES at PCI Gen4 Data Rate



16G TX Eye with Jitter Breakdown



RX Jitter Tolerance @ 16G

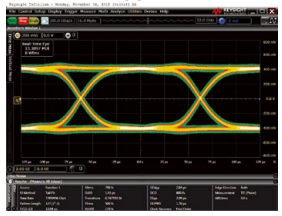
- Flawless first silicon
- Passing PRBS in both internal and external loopback modes for 2.5G, 3G, 5G, 6G, 8G, 10G, 15G, 16G, 20G, 24G speeds

Data Rate (Gbps)	Total Power (mW/lane) (min / typ / max)	Power (mW/Gbps/lane) (min / typ / max)
5	27.05 / 34.28 / 42.54	5.41 / 6.86 / 8.51
8	39.40 / 48.58 / 61.42	4.92 / 6.20 / 7.68
16	52.17 / 68.52 / 86.56	3.26 / 4.28 / 5.41

PCI Express Power Measurements

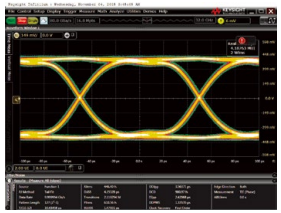
Silicon Measurement
5G to 22G Speeds with No Frequency Holes

5G

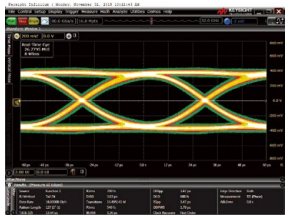


8G

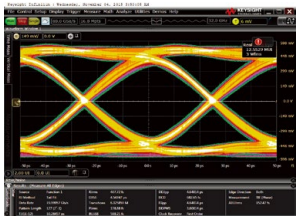
10G



16G



20G



22G

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Conclusion

- Half Power SERDES at PCI Gen4 Data Rate
- Silicon-proven in TSMC's 16nm FFC
- Performance characterized with AFS Platform enabling
  - Rapid and accurate block-level and top-level analysis
  - Good simulation-to-silicon correlation
  - Leveraging full-spectrum device-noise analysis technology
- MGC-TSMC Device Noise Analysis Flow provided good results with excellent run-times
- Future work : AFS TMI2 based Aging Simulation

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Acknowledgements

- Nandu Bhagwan - Analog Bits
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